EE 332 Laboratory Final Design Project

"Variable Gain Amplifier with Output Stage Optimization for Audio Amplifier Applications"

Instructor: Tai-Chang Chen

Due dates:

1. Operation of the circuit should be verified by your lab TA by Friday, 08/10 5pm. You are responsible for scheduling an appointment with the TA.
2. Design documentation must be submitted to the TA by Friday, 08/10 5pm.

Grading of the project:

1. Demonstration of the circuit operation in the lab (50 points)
2. Complete design documentation (50 points)
3. Extra credits (10 points)

Overview:

This design project aims to utilize every single skill you have learned in EE 332 this quarter. You will use your newly acquired knowledge to build a useful product that could potentially be subsequently refined and sold. This is the second step, after marketing, of a typical commercial production process: creating a working prototype.

Your job is to produce an audio amplifier that can take the input from a CD player or portable music player and amplify the signal to drive a loudspeaker. Your design can utilize any passive electronic components, discrete BJT's or/and MOSFET's (array chips are okay too). Listed below are some project specifications as well as the equipment that is available to you:

Input signal specifications:
Signal voltage: 100mV pkpk (min) – 5.6V pkpk (max)
Signal source resistance 50 Ω
Equipment available for testing:
Hardware: Oscilloscope, DMM, Signal generator, power supply +/-10 V DC
Software: multisim, PSPICE, HSPICE etc.

Minimum Design Specifications of the amplifier:
Output power: 0.5W (minimum)
Load Impedance (speaker): 8Ω
Idling power: < 1W
Distortion: No audible distortion in casual listening

Extra credit
Bandwidth: 20Hz to 20K Hz

Design Description:
A skeleton description of what your design may look like is as follows:
Your amplifier will take a small signal input from a music player, and then presumably send it into a gain stage to meet the gain requirements for the design. As you have learned, we will need a specially designed output stage to drive a speaker resistance of 8 ohms.

As you may have noticed, the input signal specifications provide a large range of input amplitudes. There are a number of reasons for this. The first is to ease requirements for simply meeting specifications, while leaving SIGNIFICANT room for optimization. Also, input signal specifications from a music source are not always easily accessible, so this will give you some flexibility to tune your amplifier to achieve good sound quality. And finally, the .5W specification may be very loud for a speaker. The flexibility of your amplifier will allow you to vary the gain for better audio quality.

Thus, the audio amplifier you design must be more flexible than audio amplifiers you are used to, since you must be able to handle a wide range of inputs, and still tune the gain to achieve .5W on the output.

**Please note that your amplifier does not have to automatically correct for a changing input size. A digital class might require a state machine or even more complicated circuit to achieve this, but you can be happy this is an analog class and a potentiometer or similar structure will work just fine.

Design Decision Justification:

There is no specific topology that you should follow, the method is open-ended and you are free to explore any resources. With this in mind, the decisions and tradeoffs you make in your design will be critical in determining the overall quality of your project, and thus will play a significant role in the final grade.

You must justify all blocks in your design. Why did you implement a given output stage? Which component did you use and why? What is the associated cost/performance tradeoff? It is encouraged to meet specifications while looking to optimize in one of the following areas: performance (output power or bandwidth), and cost. This is a great opportunity to design something that is truly yours, so use it that way.

Optimization:

There is much room for improvement to *exceed* the specifications. Please aim to meet the specifications first (it may not be as easy as you think!), and then look to optimize an aspect of your design.

Timeline:

You are highly encouraged to start early. I anticipate that this will take about three weeks of about 6-10 hours each to complete, including simulation and testing. In order to guide you through this process, I have setup milestones to help you maintain the momentum.

Project Report Requirements

Introduction

- Briefly explain the objective of the project

Architecture Design

- Design specifications
- Block Diagrams
- Discussion on the chosen architecture
- Trade offs

Circuit Design

- Schematics
- Design equations and calculations
- Simulation results

Assembly and Testing

- Notes on assembly process
- Description of testing process and results
- Notes on any design changes implemented

Results

Maximum Output Power

- What is the largest Vpk-pk on output that is not distorted/clipping and greater than or equal to .5W

Idling power

- DC power used with no input

Cost/Parts Count

- How many op-amps did you use?
- Count up total parts and submit cost

Grading:

Report: 50%

Demonstration: 50%

Functionality: 20%

Justification: 30%

Weekly Progress Recommendations

Week 1:

- Circuit Topology Determined
- Try to get all stages connected and simulated
- At LEAST 1 stage built, tested

Week 2:

- All stages built
- You should now be working to finalize optimizations

Week 3:

- Class Demo in EE 137
- Final project report turn in